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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/754,835	01/09/2004	Min-Hsiung Chiang	TS02-1398	9791

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/754,835	CHIANG, MIN-HSIUNG	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election without traverse of claims 19-27 in the reply filed on 3/28/05 is acknowledged.

2. The abstract of the disclosure is objected to because the abstract should describe the structure of the device instead of the method to make the device. Correction is required.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The disclosure is objected to because of the following informalities: It is believed that the reference numeral for the heavily doped source/drain region is "16" instead of "19" (page 11, line 12).

Appropriate correction is required.

5. Claims 19 and 22 are objected to because of the following informalities: Claim 19, line 4, the phrase "the top surface" has no antecedent basis. Claim 22, line 1, the phrase "the depth" has no antecedent basis. Appropriate correction is required.

6. Claims 19-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19, line 5, the phrase "a top surfaces" is vague and indefinite. Fig. 10 discloses a second section of said STI region [6] features a top surface recessed below the top surface of said semiconductor substrate [1]. Therefore, it is recommended that the phrase should rewrite as "a top surface".

Claim 19, line 11, the phrase "semiconductor substrate" is unclear whether it is being referred to the semiconductor substrate in line 3 of claim 19.

Claim 19, line 11, the phrase "recessed, said second STI section" is vague and indefinite. Is it being referred to "said second section of said STI region"?

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 19, 23 and 24 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (in the IDS filed on 3/29/04)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regards to claim 19, Huang et al. show all the elements of the claimed invention in fig. 9. It is a capacitor device [71], comprising: an insulator filled shallow trench isolation (STI) region [26] comprised with tapered sides, on a semiconductor substrate [10], wherein a first section of said STI region (a portion of region [26] formed under a region

[36]) features a top surface located at a higher level than a top surface of said semiconductor substrate, and wherein a second section of said STI region (a portion of region [26] formed under a middle portion of region [37]) features a top surface recessed below the top surface of said semiconductor substrate exposing an adjacent portion of said semiconductor substrate, wherein said adjacent portion of said semiconductor substrate features a smooth top surface and a tapered side; an insulator layer [24] lining all surfaces of said insulator filled STI region; a capacitor dielectric layer [31'] on said smooth top surface, and on said tapered side of said portion of said semiconductor substrate located adjacent to said second section of said STI region; a capacitor region [34] in said semiconductor substrate located underlying said capacitor dielectric layer; a conductive structure [37] comprised with a first portion located on said capacitor dielectric layer, and with a second portion located on a portion of said first section of said insulator filled STI region; and a silicide layer (a darkened region formed on top of layer [37]) located on a top surface of said conductive structure.

It is inherent that the silicide layer is a metal silicide layer because all silicide layers comprises metal.

In regards to claim 23, Huang et al. further disclose the insulator in said insulator filled STI region [26] is silicon oxide.

In regards to claim 24, Huang et al. further disclose said capacitor region [34] is located either in an N type or P type region.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 20-22 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al.

In regards to claim 20, Huang et al. differ from the claimed invention by not showing said tapered sides of said insulator filled STI region are at an angle between about 70 to 89 degrees in relation to a horizontal top surface of said semiconductor substrate.

It would have been obvious for the tapered sides of said insulator filled STI region are at an angle between about 70 to 89 degrees in relation to a horizontal top surface of said semiconductor substrate because it depends on the desired capacitance of the capacitor.

In regards to claim 21, Huang et al. disclose said insulator layer [24], lining the surface of said insulator filled STI region, is a silicon oxide layer that contains nitrogen.

Huang et al. differ from the claimed invention by not showing the insulator layer has a thickness between about 50 to 300 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the insulator layer has a thickness between about 50 to 300 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 22, Huang et al. differ from the claimed invention by not showing the depth of recess in said second section of said insulator filled STI region, below the top surface of said first section of said insulator filled STI region, is between about 1000

to 3500 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the depth of recess in said second section of said insulator filled STI region, below the top surface of said first section of said insulator filled STI region, is between about 1000 to 3500 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 25, Huang et al. differ from the claimed invention by not showing said capacitor dielectric layer is a silicon dioxide layer, at a thickness between about 10 to 100 Angstroms.

It would have been obvious for the capacitor dielectric layer is a silicon dioxide layer because it is a conventional capacitor gate dielectric material.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the capacitor dielectric layer has a thickness between about 10 to 100 Angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 26, Huang et al. discloses the conductive structure [37] is a polysilicon structure.

Huang et al. differ from the claimed invention by not showing the conductive structure is a doped polysilicon structure. It would have been obvious for the conductive structure is a doped polysilicon structure, since it has been held to be within the general

skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416. In addition, doped polysilicon would reduce the resistance of the capacitor electrode.

In regards to claim 27, Huang et al. differ from the claimed invention by not showing said metal silicide layer is comprised of either titanium silicide, tantalum silicide, cobalt silicide, nickel silicide or zirconium silicide.. It would have been obvious for said metal silicide layer is comprised of either titanium silicide, tantalum silicide, cobalt silicide, nickel silicide or zirconium silicide., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. In re Leshin, 125 USPQ 416.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 29, 2005

Steven Loke
Primary Examiner